CLAIMS

What is claimed is:

1. A shallow trench isolation region formed in a layer of semiconductor material, comprising:

a trench formed in the layer of semiconductor material, the trench being defined by sidewalls and a bottom;

a liner within the trench formed from a high-K material, the liner conforming to the sidewalls and bottom of the trench; and

a fill section made from isolating material, and disposed within and conforming to the high-K liner.

2. The isolation region according to claim 1, wherein the high-K material has a compressive stress to compress an adjacent active region disposed in the layer of semiconductor material and defined by the shallow trench isolation region, and the active region having a semiconductor device formed therefrom, the compressive stress effective to enhance electron mobility within the active region.

3. The isolation region according to claim 2, wherein the semiconductor device is an NMOS device.

4. The isolation region according to claim 1, wherein the high-K material has a tensile stress to strain an adjacent active region disposed in the layer of semiconductor material and defined by the shallow trench isolation region, and the active region having a semiconductor device formed therefrom, the tensile stress effective to enhance hole mobility within the active region.

5. The isolation region according to claim 4, wherein the semiconductor device is a PMOS device.

6. The isolation region according to claim 1, wherein the fill section is composed of one or more materials selected from silicon oxide, silicon nitride, polysilicon and mixtures thereof.

7. The isolation region according to claim 6, wherein the fill section is deposited using chemical vapor deposition (CVD).

8. The isolation region according to claim 1, wherein the layer of semiconductor material is a semiconductor film disposed on an insulating layer, the insulting layer being disposed on a semiconductor substrate.

9. The isolation region according to claim 8, wherein the bottom of the trench is defined by the insulating layer.

10. A method of forming a shallow trench isolation region in a layer of semiconductor material, comprising:

forming a trench in the layer of semiconductor material, the trench having sidewalls and a bottom;

forming a layer of high-K material, the layer of high-K material conforming to the sidewalls and the bottom of the trench to line the trench with a high-K liner; and

filling the high-K material lined trench with an isolating material.

11. The method according to claim 10, further comprising forming a semiconductor device using an active region disposed in the layer of semiconductor material and defined by the shallow trench isolation region, wherein the high-K material has a compressive stress to compress the active region, the compressive stress effective to enhance electron mobility within the active region.

12. The method according to claim 11, wherein the semiconductor device is an NMOS device.

13. The method according to 10, further comprising forming a semiconductor device using an active region disposed in the layer of semiconductor material and defined by the shallow trench isolation region, wherein the high-K material has a tensile stress to strain the active region, the tensile stress effective to enhance hole mobility within the active region.

14. The method according to claim 13, wherein the semiconductor device is a PMOS device.

15. The method according to claim 10, wherein the fill section is composed of one or more materials selected from silicon oxide, silicon nitride, polysilicon and mixtures thereof.

16. The method according to claim 15, wherein the fill section is deposited using chemical vapor deposition (CVD).

17. The method according to claim 10, wherein the layer of semiconductor material is a semiconductor film disposed on an insulating layer, the insulting layer being disposed on a semiconductor substrate.

18. The method according to claim 17, wherein the bottom of the trench is defined by the insulating layer.